

Remarks:

Reconsideration of the application, as amended herein, is respectfully requested.

Claims 1 - 11 and 13 - 18 are presently pending in the application. Claims 1, 2, 3, 6, 7, 11, 13 and 16 have been amended. Claim 12 has been canceled. New claim 18 has been added.

In item 3 of the above-identified Office Action, claims 8, 9 and 16 were rejected as allegedly being indefinite under 35 U.S.C. § 112, second paragraph. More specifically, it was alleged in item 4 of the Office Action that the limitation "units" in line 4 of claims 8 and 16 lacked sufficient antecedent basis. Claim 1 has been amended to recite, among other things, "units", thus providing proper antecedent basis for the use of "units" in claims 8 and 9. Additionally, claim 16 has been amended herein to address the concerns raised in items 3 and 4 of the Office Action.

Support for the amendment to claim 16 can be found in the specification of the instant application, for example, on page 16, lines 6 - 13, which states:

When the programmable unit is intended to continue running once again after stopping and debugging, the signal SUSPEND which was supplied to the stopping delay apparatus DEL is set to the value 0, which

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results in the flip-flop FF being reset and a signal
SUSPEND = 0, **which no longer stops the peripheral
units P1 and P2**, being emitted from the stopping delay
apparatus DEL, **and the stopping of the running of the
program by the program running units is then
cancelled.** [emphasis added by Applicant]

It is accordingly believed that the claims meet the
requirements of 35 U.S.C. § 112, second paragraph.

In item 6 of the Office Action, claims 1, 10, 11 and 17 were
rejected under 35 U.S.C. § 102(e) as allegedly being
anticipated by U. S. Patent No. 6,349,392 to Swoboda et al
("SWOBODA").

In item 11 of the Office Action, claims 1 - 7 and 10 were
rejected under 35 U.S.C. § 103(a) as allegedly being obvious
over European Patent No. 0 455 946 A2 to Harrison
("HARRISON"). In item 20 of the Office Action, claims 8 and 9
and 10 were rejected under 35 U.S.C. § 103(a) as allegedly
being obvious over **HARRISON**, in view of U. S. Patent No.
5,956,514 to Wen et al ("WEN"). In item 23 of the Office
Action, claims 11 - 15 and 17 were rejected under 35 U.S.C. §
103(a) as allegedly being obvious over **HARRISON**, in view of
SWOBODA. In item 25 of the Office Action, claim 16 was
rejected under 35 U.S.C. § 103(a) as allegedly being obvious
over **HARRISON**, in view of **SWOBODA** and **WEN**.

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Applicant respectfully traverses the above rejections, as applied to the amended claims.

More particularly, claim 1 has been amended to recite, among other limitations:

other components connected to said stopping device, said stop command causing said other components to be stopped, in addition to stopping said program operation unit with which said stopping device is associated, said other components including units which are connected to and cooperate with said program operation unit; and

a delay apparatus which, in response to receipt of said stop command, deliberately delays the stopping of said units until after the stopping of said program operation unit. [emphasis added by Applicants]

Similarly, Applicant's claim 11 has been amended to recite, among other limitations:

peripherals which are not program operation units, connected to said stopping device, said stop command causing said peripherals to be stopped, in addition to stopping said at least one program operation unit with which said stopping device is associated, said peripherals being stopped in response to said stop command after a deliberate delay so that said peripherals are stopped after said at least one program operation unit is stopped. [emphasis added by Applicant]

The amendments to Applicant's independent claims are supported by the specification of the instant application, for example, in paragraphs [0040], which states:

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The peripheral units P1 and P2 are stopped by the first OCDS module OCDS1 emitting a signal SUSPEND=1. The suspend signal SUSPEND is emitted, for example, at the time at which the program running units CORE1 and/or CORE2 are stopped, and is supplied to the stopping delay apparatus DEL. The stopping delay apparatus DEL passes the signal on, with a specific delay, to the peripheral units P1 and P2, and in consequence stops them. The delaying of passing on of the SUSPEND signal to the peripheral units P1 and P2 results in that they are not stopped until a certain amount of time has passed from the time at which the program running units were stopped. [emphasis added by Applicant]

Paragraphs [0047] - [0048] of the instant application disclose certain advantages, among others, that result from the delayed stopping of the peripheral units. More particularly, paragraphs [0047] - [0048] of the instant application, state:

As is easy to comprehend, the stopping delay apparatus DEL emits a SUSPEND signal (SUSPEND=1), which stops the peripheral units P1 and P2, only when it is supplied with a signal SUSPEND=1, and all the signals BUSY from the program running units CORE1 and CORE2 (and/or from the interfaces MIF1 and MIF2 associated with them) as well as from the bus bridge BB have the value 0.

The delayed stopping of the peripheral units P1 and P2 gives the program running units CORE1 and CORE2, or other bus masters, the opportunity to carry out other write or read access operations, which have already been started or have been defined at the time when program running was stopped (for example to empty what is referred to as the write-back buffer in the program running units). This has been found to be advantageous since, in consequence, the debugging process which follows the stopping of the programmable unit is itself simplified and provides more reliable results on the present state of the programmable unit, and since the programmable unit is in this way changed to a state which ensures that the programmable unit will continue processing correctly once the stop state has been cancelled (that is to say it will continue

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processing as it would have done if it had not been stopped). [emphasis added by Applicant]

None of the cited references teach or suggest, among other limitations of Applicant's claims, in response to a stop command, deliberately delaying the stopping of certain units (i.e., peripherals or other units) until **after** a program operation unit has been stopped, as currently claimed by Applicant.

More particularly, Applicant's claim 4 and former claim 12 claims recited, among other limitations, stopping the peripherals/units "**later in time**" from the program operation unit. The Office Action did not apply the **SWOBODA** reference, by itself, against Applicant's claim 4 and former claim 12, including the "later in time" limitation. Rather, in connection with Applicant's claims 4 and 12, the Office Action alleged that **HARRISON**:

. . . has taught the programmable unit of claim 3, wherein said units are stopped by said stopping device later in time than said program operation unit and said further program operation unit: [The processors (P1-P7) can be selectively stopped, depending on the settings within bus monitor 12. The settings are alterable, i.e., **the bus monitor can be set up to issue stop commands to certain processors at one point during processing, then the set-up can be altered so that different processors are issued stop command.** [Fig. 5, and col. 9, lines 17 - 35] Therefore, some units (e.g., PO 3 and 4) can be initially not given the stop command **upon a first breakpoint**. Then, the bus monitor 12 can be reconfigured so that **upon another breakpoint (later in time)**, the units (PO 3

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and 4 will be issued a stop command.] [emphasis added
by Applicant]

As can be seen from the argument made in the Office Action, in order to use **HARRISON** to allege that the other units are stopped "later in time" a plurality of separate and different breakpoints (i.e., a first breakpoint; another breakpoint) must be issued. Contrary to the teaching of **HARRISON**, Applicant's currently claimed invention stops both the processor and the other units in response to a single stop command, however, Applicant's claims require, among other things, that in response to the stop command, the stopping of the peripherals/units be deliberately delayed until after a program operation unit has stopped. Certain of Applicant's dependent claims further define this **deliberate delay**, for example, to be determined, in part, by whether another component in the system has no more data to pass on. See, for example, dependent claims 14, 15 and 18.

However, neither **SWOBODA**, nor **HARRISON**, teach or suggest, in response to a stop command, stopping a program operation unit and certain other peripherals and/or units, and deliberately delaying the stopping of the other peripherals/units until after the program operation unit has stopped. The **WEN** reference, cited in combination with **HARRISON** and/or **HARRISON** and **SWOBODA** against certain of Applicant's dependent claims,

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does not cure the above-discussed deficiencies of **SWOBODA** and **HARRISON**.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 1 and 11. Claims 1 and 11 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1 or 11.

In view of the foregoing, reconsideration and allowance of claims 1 - 11 and 13 - 18 are solicited.

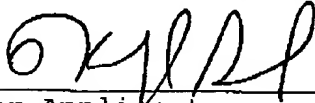
In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

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Respectfully submitted,



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